REMARKS/DISCUSSION OF ISSUES

Applicant thanks the Examiner for his many courtesies extended during the interview of March 23, 2005. While no final agreement was reached, Applicant is confident that progress was made and that both Examiner and Applicant understand the position of their opposite better than prior to the interview.

New claims 37-40 are patentable over the prior art as the prior art fails to disclose, teach, or suggest each and every element of those claims. Support for new claims 37-40 can be found, inter alia, on page 5 of the specification of *United States Patent Application 10/664,455.*

Replacement drawings obviating the Examiner's objection are attached hereto.

Claims 21-24, 28-30, and 33-35 were rejected as unpatentable over Farrell under 35 U.S.C. §103(a). This rejection is traversed.

In order to maintain this §103(a) rejection, each and every element of the claims must be taught or suggested in at least as great detail as claimed. As Farrell does not teach use of address bit signals as being indicative of cache configurations, as claimed in claims 21, 23, 28, 33, and 34, this rejection must fail.

At most, Farrell teaches that input cache configuration signals 28 and tag field bits 16a provide decoded enable signals. However, cache configuration signals 28 are not address bit signals, as the cache configuration signals 28 are sent from the select logic 38 to a cache controller signal, rather than to the pins. "[p]in 22a and pin 26b are electrically coupled via a conductor to concurrently receive a second address bit signal." *See, specification of United States Patent Application 10/664,455 at page 5.* Since the cache configuration signals of Farrell are not sent to the conductor, and instead are sent to a cache controller chip 24, (see FIG. 2 of Farrell) Farrell cannot render these claims unpatentable. It should be noted that Applicant is *not* arguing based on unclaimed material – Applicant is arguing that the claimed "address bit signals" are not the same signals as Farrell's input cache configuration signals and tag field bits.

Additionally, the Examiner's statement that it was well known that operating systems at the time of the invention used their BIOS to initialize memory upon startup is not relevant to whether these claims are patentable, and this statement is specifically traversed. That "memory configuring upon startup was very well known in the art" and "it would have allowed the data processing system to know what memory was available and to determine how it should be utilized" do not address whether the claimed elements are taught or suggested by the reference. Indeed, a modification as suggested by the Examiner precisely illustrates why the claimed invention is *not* obvious. The Examiner's argued modification does not arrive at the claimed invention, and instead merely presumes the BIOS knows to select between multiple memory cache configurations. Such a presumption destroys the principle of operation of the reference, in contravention of the strictures of §103(a), as the reference uses the multiplexor based on four hit signals and input cache configuration signals and two tag field bits. See, column 5, lines 13-15.

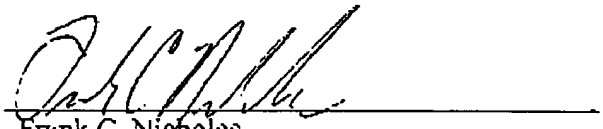
Withdrawal of the rejections to claims 21-24, 28-30 and 33-34 is requested.

CONCLUSION

The Applicant respectfully submits that claims 21-24, 28-30 and 33-34 as listed herein fully satisfy the requirements of 35 U.S.C. §§102, 103 and 112. New claims 37-40 are allowable. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested.

Dated **May 20, 2005**

Respectfully submitted,
Keenan W. Franz, *et al.*



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